Design and Performance of a Highly Integrated Wideband Active Downconverter MMIC

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***Abstract* — The design and performance of a highly integrated wideband downconverter MMIC is described. The circuit utilizes 0.25μm pHEMT technology and a high density interconnect (HDI) process to yield a single ended, double balanced active downconverter with a 1mm^2 die area. The circuit is self biased and draws 17-24mA from a single 3-5V positive supply. Diode level shifting is employed to achieve a direct coupled IF output. Measured performance of the MMIC demonstrates 10GHz 3dB-RF bandwidth and positive conversion gain through 18GHz.**

I. Introduction

High performance, low power downconverters are extensively employed in mobile, base station and satellite communication systems. A compact, fully integrated MMIC solution will support low cost, high volume production and system integration. This paper describes the design and performance of a highly integrated, low power, active downconverter MMIC. A high density interconnect (HDI) process and 0.25μm MMW-pHEMT technology are utilized to yield a circuit that consumes only 1mm^2 of GaAs real estate. Active RF/LO baluns, FET mixer core, and IF combiner circuits are integrated on-chip such that no external matching, combining or filter networks are required for single ended double balanced operation. Performance summaries for some key wideband downconverter references are listed in Table I.

TABLE I
STATE OF THE ART WIDEBAND DOWNCONVERTER MMICS

Reference / Parameter	[1]	[2]	[3]	This Work
Conv. Gain (dB)	10.0	15.3	10.0	15.2
3dB-RF BW (GHz)	10	20	8	10
DC Power (mW)	---	1440	90	120
Supply Voltage (V)	---	-6	+9	+3 to +5
LO Power (dBm)	~ 0	10	0	0
Die Area (mm^2)	5.00	1.26	1.00	1.00
Single Ended	Yes	No	Yes	Yes
Device Technology	0.2 μm MESFET	InP HBT	GaAs HBT	0.25 μm pHEMT

The results presented in this paper represent an increase in conversion gain with respect to [1] and [3], and a decrease in DC power consumption in comparison to [2].

II. HDI Process Description

The fabrication process combines high performance dual-recess 0.25μm pHEMT devices with high density interconnect metalization. The active device fabrication sequence is a follows:

- Ohmic contact metalization and alloy
- Isolation by implantation
- First channel recess using optical lithography and combined plasma and wet chemical etching
- Gate fabrication using direct-write e-beam, wet etch to etch stop layer, Ti/Pt/Au metal evaporation, and liftoff

The passive device fabrication sequence is:

- 500Å Nitride0 deposition
- 50Ω/sq. TaN resistor deposition by sputtering
- Metal0 deposition by evaporation and liftoff
- 2000Å Nitride1 deposition
- Metal1 deposition using a sputtered field metal followed by electroplate
- 500Å Nitride2 deposition
- MIM capacitor top plate metalization by evaporation and liftoff
- Air Bridge photoresist pattern
- Metal2 deposition using a sputtered field metal followed by electroplate
- Protective Overcoat (PO) nitride deposition

All nitride layers are deposited by PECVD and etched by RIE, resulting in minimal etch undercut. The frontside process is followed by wafer thinning to 100μm and conventional GaAs MMIC backside processing, including 40μm diameter plated-through via holes and electroplated gold backside metalization. A number of MIM capacitor structures are technically possible using this sequence, and four are allowed in practice:

1. Ohmic-Nitride0-Metal0 ⇒ 1200 pF/mm^2
2. Metal0-Nitride1-Metal1 ⇒ 300 pF/mm^2
3. Metal0-Nitride2-MIM ⇒ 1200 pF/mm^2
4. Metal0-Nitride1-Nitride2-MIM ⇒ 240 pF/mm^2

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Capacitor types 1 and 3 can be "stacked" and connected in parallel to achieve a total capacitance density of 2400 pF/mm^2. An SEM of a stacked capacitor is shown in Fig. 1. The active downconverter MMIC makes extensive use of stacked capacitors as DC blocks. Interconnect layer properties for the HDI process are summarized in Table I.

TABLE I
HDI INTERCONNECT LAYERS

HDI Layer Name	Minimum Linewidth / Spacing (μm)	Layer Thickness (μm)	Electrical Properties
Ohmic	2 / 2	0.3000	Max 1.0 mA/μm
Nitride0	2 / 2	0.0500	1200 pF/mm^2
TaN	2 / 2	0.0600	50 Ω/sq.
Metal0	2 / 2	0.7700	Max 1.6 mA/μm
Nitride1	2 / 2	0.2000	300 pF/mm^2
Metal1	2 / 2	2.0000	Max 4.8 mA/μm
Nitride2	2 / 2	0.0500	1200 pF/mm^2
MIM	4 / 2	0.7700	Max 1.6 mA/μm
Metal2	4 / 4	4.0000	Max 9.6 mA/μm
PO	7 / 7	0.2000	Overcoat

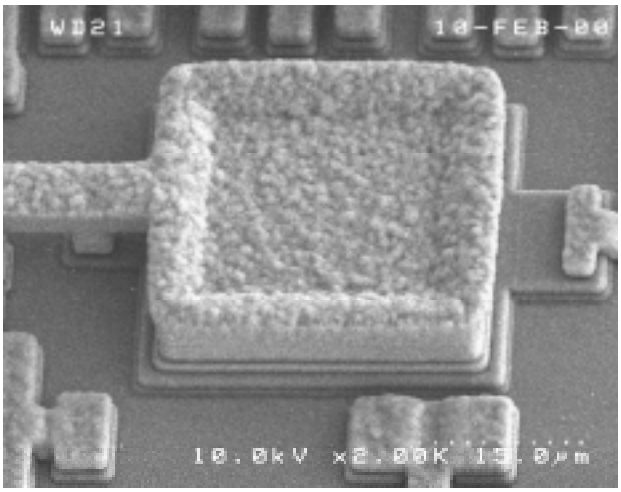

Fig. 1. SEM of fabricated stacked capacitor structure. The metal trace on the left contacts top and bottom plates; the right-hand trace contacts the middle plate.

III. CIRCUIT DESIGN

The requirement for wide bandwidth and low power consumption motivated the utilization of 0.25μm pHEMT technology. High transconductance under low current bias conditions permits the use of wideband resistive matching circuits. A simplified schematic of the downconverter MMIC is shown in Fig. 2, and a photograph of the fabricated device is shown in Fig. 3. The die dimensions are 1mm x 1mm, and the circuit may be on-wafer RF-probed.

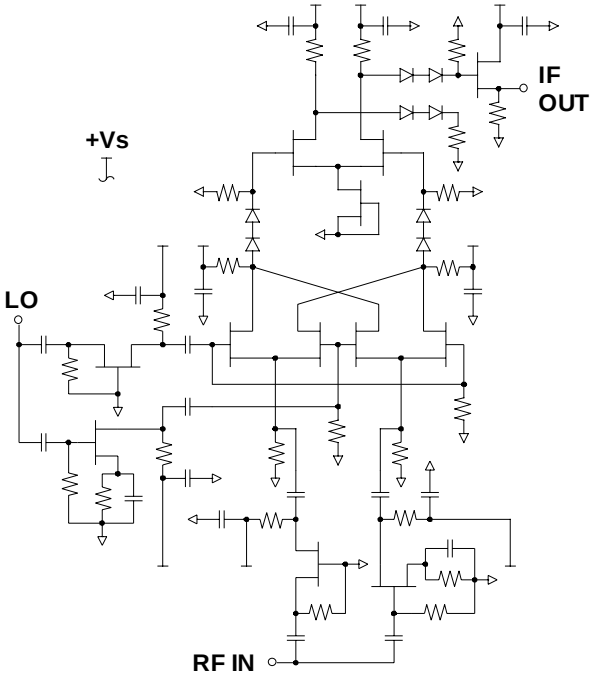

Fig. 2. Simplified schematic for the downconverter MMIC. On-chip supply bus connections are not shown.

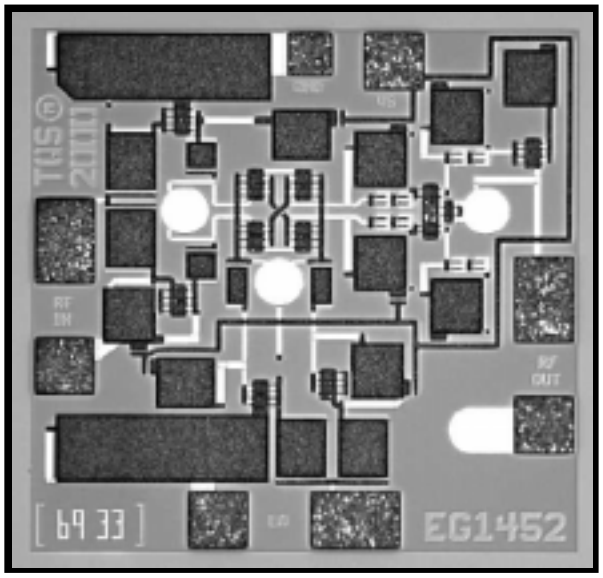

Fig. 3. Photograph of the fabricated downconverter MMIC.

Active balun, mixer and combiner topologies were selected to minimize circuit size. The RF and LO balun circuits are parallel connected common source and common gate amplifiers [4]. This topology provides a good input impedance match and the required differential signal split. The double balanced mixer core is a variant of the conventional FET Gilbert cell circuit, modified for low voltage operation by replacing the RF buffer FETs with resistors [5]. These resistors also provide a self biasing function as well as feedback to help minimize the effect of device mismatch. The IF output signals extracted from the drains of the mixer core FETs are combined with a differential amplifier circuit [6]. One output of the differential pair drives a source follower which provides a wideband output impedance match for the MMIC. Diode level shifting is used for both the differential amplifier and source follower to achieve a direct coupled IF output.

IV. Measured Results

After completion of backside processing the circuits were 100% tested on-wafer at TriQuint's production RF-probe facility. Results for the conversion gain at a 2GHz lower sideband RF and 0.5GHz IF are shown in Fig. 4. A mean conversion gain of 14.9 dB with a standard deviation of 0.6 dB was observed for 3457 devices from the 4 wafer process lot.

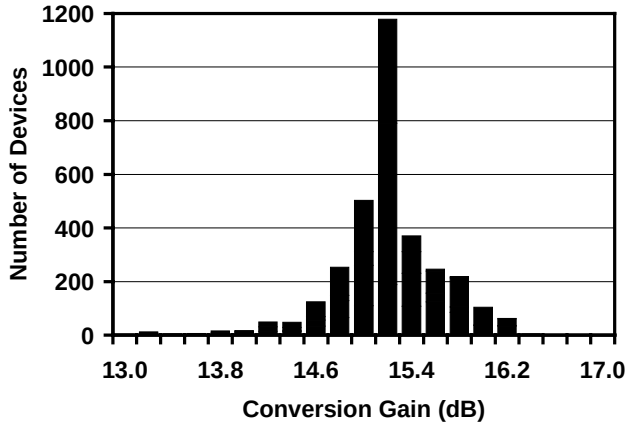

Fig. 4. Measured on-wafer conversion gain, +5V, -5dBm LO power, LSB 2GHz RF, 0.5GHz IF.

Separated devices were soldered to carrier plates and bond wire connected to 50Ω microstrip transmission lines for in-fixture testing. SMA launchers were used to provide an interconnect to the microstrip lines. The only external component used for the measurements was a 0.01μF capacitor to bypass the supply line. Typical DC power consumption for the MMICs was observed to be 120mW and 51mW for supply voltages of +5.0V and +3.0V respectively.

The measured conversion gain and LO isolation are plotted in Fig 5. For a +5.0V supply and 0.5GHz IF, the measured conversion gain ranged from 15.2dB at 2GHz RF to 7.6dB at 18GHz RF. A similar RF frequency response was observed for the +3.0V supply with an approximate 3dB reduction in gain. The 3dB-gain RF bandwidth was approximately 10GHz for both supply voltages. The conversion gain rolls off rapidly for RF input frequencies below 0.2GHz due to the DC blocking capacitors used in the RF/LO baluns. Better than 25dB LO rejection was observed over the 0.2-18GHz band.

The measured IF frequency response for the downconverter is shown in Fig. 6. Positive conversion gain was measured through 4GHz for the +5.0V supply condition. The data plotted in Fig. 7 characterizes the single sideband noise figure, output 3rd order intercept point and power at 1dB conversion gain compression for the MMIC. The SSB noise figure is about 10dB up to 6GHz and has a frequency response that is nearly the inverse of that of the RF conversion gain. The output P1dB was observed to be a strong function of supply voltage due to the reduced voltage swing available for the IF stage FETs under the +3.0V supply condition. The reduction in P1dB that occurs at low frequencies is caused by the upconverted signal two-tone driving the IF stage along with the downconverted signal.

Conversion gain versus LO drive power is plotted in Fig. 8. Note that at 2GHz an LO power of –10dBm is sufficient to produce near saturated conversion gain, however, above 10GHz a 0dBm LO drive is required for optimum performance. Plotted in Fig. 9 is the measured IF, RF, and LO port return loss for the MMIC.

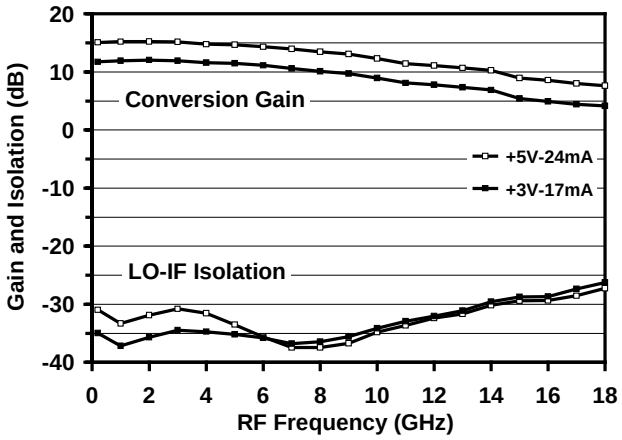

Fig. 5. Measured in-fixture conversion gain and LO to IF isolation, 0dBm LO power, LSB RF, 0.5GHz IF.

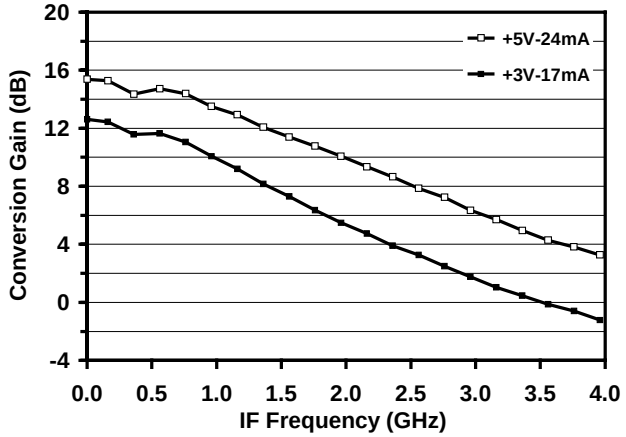

Fig. 6. Measured in-fixture IF frequency response, 0dBm LO power, LSB 4GHz RF.

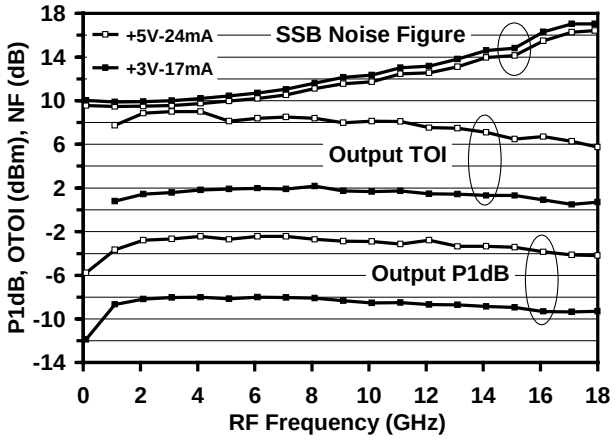

Fig. 7. Measured in-fixture output P1dB, TOI and single sideband noise figure, 0dBm LO power, LSB RF, 0.2GHz IF for noise figure and 0.5GHz IF for P1dB and OTOI.

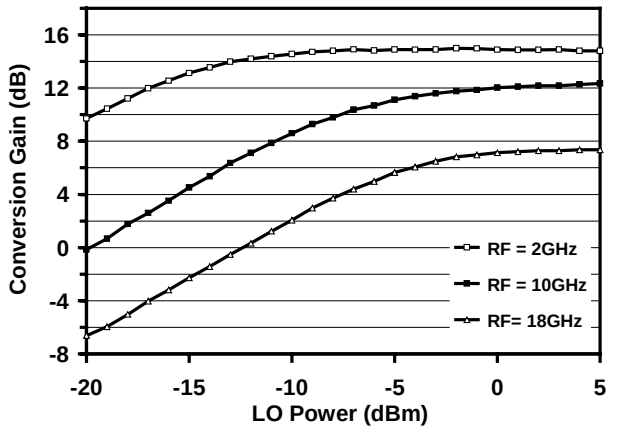

Fig. 8. Measured in-fixture conversion gain versus LO power, +5V-24mA, LSB RF, 0.5GHz IF.

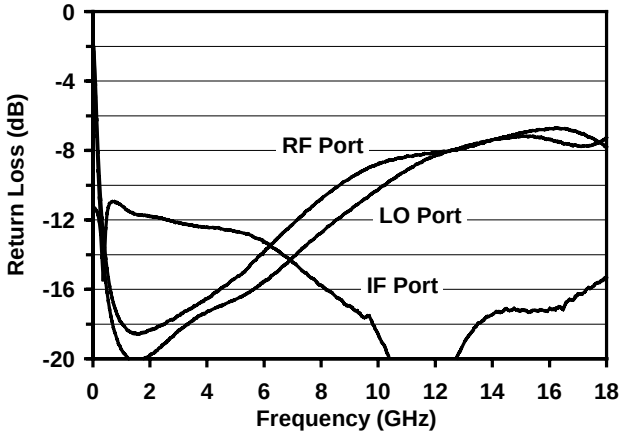

Fig. 9. Measured in-fixture return loss, +5V-24mA.

V. Conclusion

The design and performance of a wideband, low power downconverter MMIC has been presented. The mixer utilizes 0.25μm pHEMT technology and a high density interconnect process to achieve a highly integrated circuit with a 1mm^2 die area. Measured +5.0V results for the device demonstrate 15.2dB conversion gain, 10GHz 3dB-RF bandwidth, 7.6dB conversion gain at 18GHz, and 120mW DC power consumption. With respect to conversion gain, bandwidth, DC power consumption, and die size; these are results are among the best reported for pHEMT downconverter MMICs.

References

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